AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (previously presented) Apparatus for processing data, said apparatus comprising:

an instruction fetching circuit operable to fetch program instructions from a sequence of memory locations;

an instruction decoder responsive to program instructions fetched by said instruction fetching circuit to control data processing operations specified by said program instructions; and

an execution circuit operable under control of said instruction decoder to execute said data processing operations;

a program counter register operable when said apparatus is executing said program instructions from said sequence of memory locations to store an address indicative of a memory location of a program instruction being executed within said program instructions from said sequence of memory locations; and

a block counter register operable to store a block count value indicative of a location of a program instruction being executed within a block of two or more program instructions,

wherein said instruction decoder is responsive to an execute block instruction to trigger fetching of a block of two or more program instructions by said instruction fetching circuit and execution of said block of two or more program instructions by said execution circuit, said block of two or more instructions containing a number of program instructions specified by a block length field within said executed block instruction and being stored at a memory location specified by a location field within said execute block instruction; and

wherein when executing said block of two or more program instructions, said program counter register is configured to store an address indicative of a memory location of said execute block instruction and said block counter register is configured to store a block count value indicative of said program instruction location of a program instruction being executed within said block of two or more program instructions corresponding to said execute block instruction,

the apparatus further comprising:

an exception handling circuit operable upon occurrence of an exception during execution of said block of two or more instructions to store said block count value, and upon completion of handling of said exception, to restart execution of said block of two or more program instructions at a program instruction within said block of two or more instructions indicated by said block count value.

2. (original) Apparatus as claimed in claim 1, wherein after execution of said block of two or more program instructions a return is made to a program instruction outside of said block of two or more program instructions.

3. (previously presented) Apparatus as claimed in claim 1, wherein said return is to a program instruction immediately following said execute block instruction within said sequence of memory locations.

4. (previously presented) Apparatus as claimed in claim 1, wherein said location field is an offset field specifying said location of said block of two or more program instructions relative to a memory location of said execute block instruction.

5-8. Canceled.

9. (currently amended) Apparatus as claimed in claim 1, wherein said exception handling circuit is operable to store ~~said~~ an address of said execute block instruction upon occurrence of said exception and to restore said address of said execute block instruction to said program counter register upon said completion of handling of said exception.

10. (previously presented) Apparatus as claimed in claim 2, wherein upon completion of execution of said block of two or more program instructions said instruction decoder is operable to return processing to a program instruction following said execute block instruction as indicated by said program counter register.

11. (previously presented) A method for processing data, said method comprising the steps of:

fetching program instructions from a sequence of memory locations with an instruction fetching circuit;

controlling data processing operations specified by said program instructions with an instruction decoder; and

executing said data processing operations with an execution circuit controlled by said instruction decoder;

storing within a program counter register an address indicative of a memory location of a program instruction being executed within said sequence of program instructions; and

storing within a block counter register a block count value indicative of a location of a program instruction being executed within a block of two or more program instructions,

wherein said instruction decoder is responsive to an execute block instruction to trigger fetching of a block of two or more program instructions by said instruction fetching circuit and execution of said block of two or more program instructions by said execution circuit, said block of two or more instructions containing a number of program instructions specified by a block length field within said executed block instruction and being stored at a memory location specified by a location field within said execute block instruction,

wherein when executing said block of two or more program instructions, said program counter register stores an address indicative of a memory location of said execute block instruction and said block counter register stores a block count value indicative of said program instruction location of a program instruction being executed within said block of two or more program instructions corresponding to said execute block instruction; and

upon occurrence of an exception during execution of said block of two or more instructions storing said block count value and upon completion of handling of said exception, restarting execution of said block of two or more program instructions at a program instruction within said block of two or more instructions indicated by said block count value.

12. (original) A method as claimed in claim 11, wherein after execution of said block of two or more program instructions a return is made to a program instruction outside of said block of two or more program instructions.

13. (previously presented) A method as claimed in claim 11, wherein said return is to a program instruction immediately following said execute block instruction within said sequence of memory locations.

14. (previously presented) A method as claimed in claim 11, wherein said location field is an offset field specifying said location of said block of two or more program instructions relative to a memory location of said execute block instruction.

15-18. Canceled.

19. (currently amended) A method as claimed in claim 11, wherein upon occurrence of said exception storing ~~said~~ an address of said execute block instruction and restoring said address of said execute block instruction to said program counter register upon said completion of handling of said exception.

20. (previously presented) A method as claimed in claim 12, wherein upon completion of execution of said block of two or more program instructions said instruction decoder is operable to return processing to a program instruction following said execute block instruction as indicated by said program counter register.

21. (previously presented) A computer program product stored on a computer-readable storage medium including a computer program operable to control a data processing apparatus having an instruction fetching circuit operable to fetch program instructions from a sequence of

memory locations, an instruction decoder responsive to program instructions fetched by said instruction fetching circuit to control data processing operations specified by said program instructions, and an execution circuit operable under control of said instruction decoder to execute said data processing operations and to store within a program counter register an address indicative of a memory location of a program instruction being executed within said sequence of program instructions;

wherein said computer program including one or more an execute block instructions is operable to trigger fetching of a block of two or more program instructions by said instruction fetching circuit and execution of said block of two or more program instructions by said execution circuit and storing within a block counter register a block count value indicative of a location of a program instruction being executed within said block of two or more program instructions, said block of two or more instructions containing a number of program instructions specified by a block length field within said executed block instruction and being stored at a memory location specified by a location field within said execute block instruction, and

wherein said one or more execute block instructions is operable to cause, during execution of said block of two or more program instructions, said program counter register to store an address indicative of a memory location of said execute block instruction and to cause said block counter register to store a block count value indicative of said program instruction location of a program instruction being executed within said block of two or more program instructions corresponding to said execute block instruction; and

exception handling code, operable upon occurrence of an exception during execution of said block of two or more instructions, to store said block count value such that upon completion of handling of said exception, execution of said block of two or more program instructions at a

program instruction within said block of two or more instructions indicated by said block count value.

22. (original) A computer program product as claimed in claim 21, wherein after execution of said block of two or more program instructions a return is made to a program instruction outside of said block of two or more program instructions.

23. (previously presented) A computer program product as claimed in claim 21, wherein said return is to a program instruction immediately following said execute block instruction within said sequence of memory locations.

24. (previously presented) A computer program product as claimed in claim 21, wherein said location field is an offset field specifying said location of said block of two or more program instructions relative to a memory location of said execute block instruction.

25-28. Canceled.

29. (currently amended) A computer program product as claimed in claim 21, wherein upon occurrence of said exception storing said address of said execute block instruction and restoring ~~said~~ an address of said execute block instruction to said program counter register upon said completion of handling of said exception.

30. (previously presented) A computer program product as claimed in claim 22, wherein upon completion of execution of said block of two or more program instructions said instruction decoder is operable to return processing to a program instruction following said execute block instruction as indicated by said program counter register.